REMARKS

Summary

In the Office Action, all pending claims are rejected. In this response, claims 6-9, 11, 12, 26, and 28 are amended, and claims 30-32 are added.

Claim Amendments

Claims 6-9, 11, 12, 26, and 28 are amended to clarify the claims, without narrowing the scope thereof.

In addition, claims 30-32 are added.

Support for the amendments can be found throughout the disclosure as filed.

Claim Rejections under 35 U.S.C. § 102

Claims 6-9, 12, 26, and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,064,114 issued to *Higgins* (hereinafter "*Higgins*"). Applicants respectfully request reconsideration of the rejections for at least the following reasons.

Claim 6 is directed to a semiconductor device including:

a carrier substrate having a bond pad;

a first microelectronic die including:

an active side and a backside,

an active side interconnect disposed on the active side and coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the backside, coupled to and in substantial vertical alignment with the active side interconnect,

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect;

an interconnect material comprising a conductive material without a wire stem, the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die electrically and directly coupled to the interconnect material.

(emphasis added). Thus, the claimed device includes a first die disposed active side facing a carrier substrate, the first die including a backside interconnect, coupled to and in substantial vertical alignment with the active side interconnect, and further including a redistributed interconnect disposed on its backside coupled with an interconnect of a second microelectronic die.

Applicants respectfully submit that *Higgins* fails to disclose the structure of claim 6. At a minimum, *Higgins* nowhere discloses a die including a backside interconnect. *Higgins* simply discloses that die 10 is disposed active side 11 facing package substrate 50 (*see Higgins*, 2:46-48; 3:42-48), but nowhere does *Higgins* even discuss a backside of die 10.

Although the Office Action asserts that *Higgins*'s substrate 50 (noted as 60 in Office Action; however, 60 refers to outer peripheral surface of *Higgins*'s substrate 50) is a microelectronic die substrate, *Higgins*'s explicitly defines its "substrate" 50 as being "a mechanical component which carries the semiconductor die and which has (i.e., supports) electrical connection from the semiconductor die to the next level of interconnection, such as through a printed circuit board." *See Higgins*, 3:42-48 (emphasis added). That is, *Higgins*'s substrate 50/60 is a carrier substrate for forming a package, such as *Higgins*'s "completed, packaged semiconductor device 1" in its Fig. 2, which may then be mounted onto a system level board such as a printed circuit board. See Higgins, 3:49-52. Moreover, had *Higgins* intended its substrate 50 to be a die, *Higgins* surely would have called it a die as *Higgins* did for its die 10.

As *Higgins* fails to disclose a backside interconnect of a die, it follows that *Higgins* cannot be said to disclose a redistributed interconnect of a backside

interconnect, disposed on a backside of a die and coupled to and offset from a backside interconnect. Similarly, *Higgins* cannot be said to disclose an interconnect material coupled directly with the redistributed interconnect.

Still further, *Higgins* cannot be said to disclose an interconnect of a second microelectronic die electrically and directly coupled to the interconnect material coupled with the redistributed interconnect of a first die. Nowhere in *Higgins*'s disclosure is a second die mentioned, explicitly or inherently. Although the Office Action asserts that die 10 (noted as 11 in Office Action; however, 11 refers to active portion of *Higgins*'s die 10) is a second semiconductor die, Higgins's die 10 is instead the only die disclosed by *Higgins*. Accordingly, *Higgins* cannot be said to disclose a first die and a second die coupled to each other via an interconnect material.

Moreover, it is uncertain how one would even include a second die to a backside of *Higgins*'s die 10 without wirebonding. *Higgins*'s die 10 does not include a backside interconnect coupled to and in substantial vertical alignment with an active side interconnect and so it is assumed that wirebonding is the only option available for practitioners of *Higgins*'s disclosure.

Accordingly, claim 6 is allowable over *Higgins* because *Higgins* fails to disclose each and every limitation of claim 6.

Claims 7-9 and 12 each depend from independent claim 6, either directly or via an intervening claim, thereby incorporating the limitations of claim 6. Thus, for at least the same reasons claim 6 is allowable over *Higgins*, claims 7-9 and 12 similarly are allowable over *Higgins*.

Claim Rejections under 35 U.S.C. § 103

1. *Higgins*: Claim 11 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Higgins*. Claim 11 depends from allowable claim 6, thereby incorporating the limitations of claim 6. Therefore, at least by virtue of its dependency,

claim 11 is patentable over *Higgins*.

2. *Higgins*/*Schueller*: Claims 28 and 29 stand rejected 35 U.S.C. § 103(a) as being unpatentable over *Higgins* in light of U.S. Patent No. 5,844,168 issued to Schueller et al. (hereinafter "*Schueller*"). Claims 28 and 29 include limitations similar to those set forth in allowable claim 6, and thus, are allowable for at least the same reasons claim 6 is allowable over *Higgins*.

Schueller fails to remedy the deficiency of Higgins. At a minimum, *Schueller* fails to disclose a die including a backside interconnect. Accordingly, *Schueller* also cannot be said to disclose a redistributed interconnect of a backside interconnect, disposed on a backside of a die and coupled to and offset from a backside interconnect. Similarly, *Schueller* cannot be said to disclose an interconnect material coupled directly with the redistributed interconnect. Still further, *Schueller* fails to disclose an interconnect of a second microelectronic die electrically and directly coupled to the interconnect material coupled with the redistributed interconnect. Instead, *Schueller* simply discloses a ball grid array structure including multiple conductive layers for providing additional circuit routing. *See Schueller*, 2:35-38.

Accordingly, claims 28 and 29 are allowable over *Higgins* even if combined with *Schueller*.

New Claims

New claims 30-32 have been added. Claims 30-32 depend from, and thus include the limitations of, claim 6. Accordingly, claims 30-32 are allowable over *Higgins*.

With regard to claim 30, said claim includes limitations directed to the second microelectronic die comprising an active side and a backside, and wherein the interconnect is disposed on the active side of the second microelectronic die. As discussed previously, *Higgins* cannot be said to disclose a second microelectronic die

coupled to a first microelectronic die via an interconnect material because *Higgins* fails to disclose a second microelectronic die.

With regard to claim 31, said claim includes limitations directed to the second microelectronic die including an interconnect disposed on both a first side and a second side of second microelectronic die, and further including a via extending from the first side to the second side to electrically couple the interconnects. *Higgins*, however, cannot be said to make such a disclosure. Even if one could characterize *Higgins*'s die 10 as a second semiconductor die (a characterization with which Applicants expressly disagree), one could not then also say that *Higgins*'s die 10 includes either (1) an interconnect disposed on both a first side and a second side of second microelectronic die, or (2) a via extending from the first side to the second side to electrically couple the interconnects.

Claim 32 depends from claim 31 and recites further limitations of the second microelectronic die further including a redistributed interconnect of a selected one of the interconnects of the second microelectronic die, wherein the redistributed interconnect is coupled to and offset from the selected interconnect. *Higgins*, however, cannot be said to make such a disclosure. As with claim 31, even if one characterizes *Higgins*'s die 10 as a second semiconductor die, one could not then also say that *Higgins*'s die 10 includes a redistributed interconnect of a selected one of the interconnects of the second microelectronic die, wherein the redistributed interconnect is coupled to and offset from the selected interconnect.

Accordingly, claims 30-32 are allowable over *Higgins*.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that claims 6-9, 11, 12, and 26-29 are in a condition for allowance. Early issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact the undersigned with any questions at either the direct-dial phone number set forth below.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 04/17/2007

/Angela M. Sagalewicz/
Angela M. Sagalewicz
Reg. No. 56,113

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: (503) 222-9981 (operator)
(503) 796-3756 (direct)